IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

K. Takahashi, et al. Atty. Dkt. 03680036AA

Serial No. Not assigned Group Art Unit: not assigned

Filed: concurrently Examiner: not assigned

For: Semiconductor Device and Method of Fabricating the same

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 C.F.R. 1.97 through 1.98 and pursuant to applicants' duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the following documents, as listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copy of the listed document is provided herewith for the convenience of the Examiner.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

If any fees are due with the filing of this Information Disclosure Statement, please charge Deposit Account No. 50-2041.

Respectfully submitted,

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Date: April 14, 2006
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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	APPLICATION NO.
03680036AA	not assigned
APPLICANT(S)	
K. Takahashi, et al.	
FILING DATE	GROUP ART UNIT
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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	BA	2003-258121	9/2003	Japan				✓
	BB	2004-152995	5/2004	Japan				✓
	BC	2004-158593	6/2004	Japan				✓

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		CA	Lee, JH, et al., "Tunable Work Function Dual Metal Gate Technology for Bulk and Non-Bulk CMOS", IEEE (2002)
		CB	Kedzierski, J., et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation", IEEE (2002

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

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U.S. PATENT APPLICATION PUBLICATIONS

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		CC	**Kedzierski, J., et al., "Threshold voltage control in NiSi-gated MOSFETs through silicidation induced impurity segregation (SIIS)", IEEE (2003)**
		CD	**Maszara, W.P., et al., "Transistors with Dual Work Function Gates by Single Full Silicidation (FUSI) of Polysilicon Gates", IEEE (2002)**

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		CE	Terai, M., et al., "Highly Reliable HfSiON CMOSFET with Phase Controlled NiSi (NFET) and Ni3Si (PFET) FUSI Gate Electrode", Symposium on VLSI Technology Digest of Technical Papers (2005)
		CF	K. Takahashi, et al., "Dual Workfunction Ni-Silicide/HfSiON Gate Stacks by Phase-Controlled Full-Silicidation (PC-FUSI) Technique for 45nm-node LSTP and LOP Devices", IEEE (2004

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